Board Layout Guidelines for EMC Control Rev C
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There are many guidelines from many sources regarding PCB layout for EMC control. They don't always agree and some are just poor advice from an EMC perspective. Note that guidelines are just that… not hard, fast rules which are always best for a given situation. With that said, here are a few of mine…

Guiding principles: Radiated EMI requires both a noise source, and antenna. The amount of radiation at a given frequency depends on the level of the noise at that frequency and the effectiveness of the antenna at that frequency.

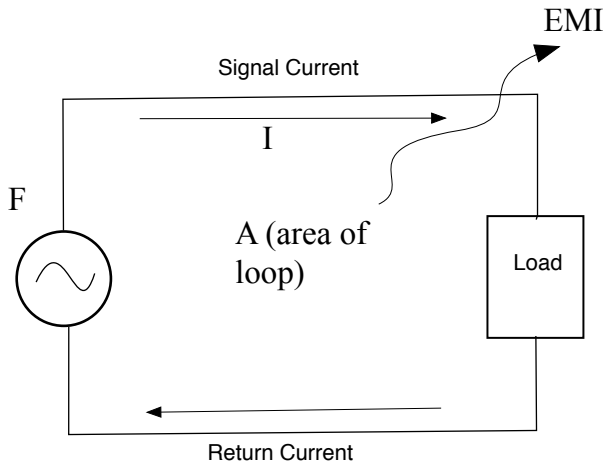
Radiated EMI can be approximated by:

$EMI = kIAF^2$ where:

EMI is radiated EMI field (v/m)
A is the area enclosed by the current path (the signal and it's return current (m^2)
F is frequency (MHz)
I is the amplitude of the current (A)
k is a proportionality constant

This relationship shows that

- Frequency is very important (as EMI varies with F^2)
- Loop Area is also very important (and relatively easy to control)
- Current (at the frequency of interest) should be minimized.



Every signal has a **return path**. Currents will always follow the path of least impedance. At the RF frequencies of EMI however, the path of least impedance is very different from the path as DC or low frequencies.

For example, for a trace routed over a ground plane, the DC return path will spread out over the plane since a wider area of copper will have a lower DC resistance than a narrower area of copper. At RF, however, the inductance of the ground plane dominates and the path of least impedance will be an image of the signal trace reflected in the plane. In other words, the return current will zig-zag directly underneath the signal trace, following it however it is routed… so long as the ground plane is *continuous* and not interrupted.

In most cases, **cables connected to the board can be the most effective antennas**, leading to the greatest EMI potential from cables rather than the board itself.

In most cases, this same concept applies to RF immunity as well as emissions.

In PCB layout, this translates into:

- Understand and minimize the loop area. This normally means paying careful attention to the return current path.
- Focus on the high frequency signals first, especially those with a high duty cycle (such as a clock line).
- Add series impedance and filtering to signals where practical (to both limit current and frequency. A slower rise time and a lower peak charging current will radiate less.
- Focus also on IO – anything connecting to or from the PCB. Coordinating the layout with shielding and filtering for each IO point is very important.

Grounding

Grounds are often thought of as equipotential… zero volts. This is not the case. Every real ground has impedance, and this impedance in very different from DC to high RF frequencies. Every current through an impedance gives rise to a voltage drop, meaning that any ground carrying current of any frequency will have a voltage variation depending on the current distribution in the ground. It is best to look at ground over a range of frequencies… DC/low; mid (ca. 1MHz); and RF (ca. 100-1000MHz).

A wire has inductance (and capacitance). At DC, a wire looks like a very low resistance by over about 10 KHz, the impedance rises quickly and the inductance dominates. At RF frequencies, the wire acts as a transmission line which has reflections depending on its terminations and reflection times depending on its length. Thus, as it approaches RF, is varies up and down in impedance reaching peaks and valleys which correspond to its series and parallel resonances (as "standing waves" develop). It can be a very effective antenna at these resonant frequencies… That is how wire antennas are designed.

Similarly, a ground plane has inductance and capacitance. At DC, the current spreads out over the surface and throughout the thickness of the plane. As frequency increases, however, the inductance begins to force the current profile to be more constrained… both in less and less spreading of the path and in the depth from the surface (the "skin effect"). At RF, the current in a plane is well constrained to mirror the signal trace routed over the plane – effectively a "microstrip" transmission line.

Though much more complex, a ground plane also can act as a resonator with standing waves and reflections. Think of a pool of water which has a disturbance such as a pebble dropping. Waves

from this disturbance propagate out from the point of disturbance. If they hit a wall, there will be a reflected wave which will in turn interact with the incident wave. Likewise, a ground plane propagates an electromagnetic wave away from the source and it reflects from any change in impedance, creating interacting waves. At a high enough frequency, standing waves which radiate efficiently could result in high common mode signals.

Experience has been that a single uninterrupted ground plane usually results in the best EMI profile. Gaps in the plane unless currents are carefully understood and managed, result in significant emissions. Tying the ground plane with multiple points (for low RF impedance) to the system metal enclosure can significantly reduce common mode nose on IO lines. I have seen this reduce emissions by 20 dB or more over an ungrounded board.

When a single ground plane is not tied directly to the case, as is often the case where a shield is used around the board, the IO lines (which will usually carry common mode noise from the GND plane) need to be either filtered (to remove the noise) or fully shielded (creating a virtual extension of the board shield). In both cases, the reference ground (to which a very low RF impedance is required) is the shield. Filters (except for common mode chokes which don't require a ground) need a very low impedance ground return to the shield and shielded cables need a direct (ideally 360° all around) terminate to the shield where it exits the shield.

Filters

"All the world is a voltage divider." In general, filters consist of a series impedance and a shunt impedance to ground. Their effectiveness depends on the series impedance being high and the shunt impedance being low at the frequencies of interest. Source impedance of a signal is important as is load impedance for a given filter to be effective. Filter components are usually characterized over frequency with a 50 ohm source and a 50 ohm load impedance. If when applied in the circuit the source and load impedances are not 50 ohms, the filter's effectiveness will be different. Further, some filters address normal mode (differential) signals, some common mode, and others both. The circuit will also have different normal mode and common mode source and load impedances, making selection all the more difficult.

With the exception of common mode chokes, which don't require a ground to function, all filters require a very good (low RF impedance) ground path for the shunt impedance element (the low side of the voltage divider). Using the correct ground and making sure it has a low RF impedance is critical. To filter a signal at it's source, the series impedance and shunt impedance should both be very close to the source. The ground return must be very low RF impedance back to the signal's source. To filter a signal as it leave the board or shield enclosure (including entering a shielded connector), the filter is located as close as possible to the exit point and the ground is the clean IO ground or shield at the exit point. Keeping a low RF impedance means low series inductance: short, wide traces, and potentially multiple connection points (e.g., PCB vias or contact fingers).

Simple ferrite beads can be very effective at adding series impedance at high frequencies while remaining low impedance to DC through MHz ranges, depending on the ferrite material. These rely on external shunt capacitance to be effective as filters.

There are many low cost 3 terminal surface mount filters in several feed-though formats. These are Tee (LCL), PI (CLC) and C (feed-though capacitor without L). Tee filters typically have a

ferrite bead in series with the input and output with a feed-though capacitor to ground in the center. Tee filters are best where source or load impedance is low or unknown. PI filters have a capacitor to ground at input and output with a series ferrite bead in between. PI filters are very effective so long as source and load impedance are high enough, but can lead to ringing with some source or load impedances. Feed-through capacitors are very effective so long as source impedance and load impedance are higher at the frequency of interest. In all cases, grounding of the filter return (the center terminal) is critical and must be a very low RF impedance to the proper ground.

There are even surface mount feed-through filters available up to 10's of amps and 100-200 V ratings (such as from API (Spectrum Control)).

Common mode chokes can be very effective for high speed differential signals such as USB data or LVDS. Common mode chokes of the correct inductance and frequency range can offer high levels of suppression of the common mode signal (i.e., present in phase on both conductors of the pair) while having minimal effect on the normal mode (differential – out of phase) signal between the pair. They function without a ground.

Data transformers, especially those with an electrostatic shield between primary and secondary, can be very good at blocking common mode noise. Note that routing of traces and planes, as well as how the shield is grounded, can defeat the effectiveness if not done correctly.

With all magnetics (ferrites, Chokes, inductors and transformers), be sure the DC or large signal current doesn't saturate the core material.

So here are some layout guidelines:

1. A continuous ground plane is almost always better than a split ground plane from an EMI perspective. Where sensitive analog signals or high power transients (such as with motors, A/Ds, and switching power supplies) must be kept separate from the ground plane, manage these paths explicitly in a different layer than the ground plane.

2. Never route a trace across a gap in the ground plane unless special attention has been paid to managing the return path. The return current for a trace routed across a gap will follow along under the trace until it hits the gap. At that point, it will follow the edge of the gap to wherever it needs to in order to mate up on the other side of the gap… creating a very large loop area in many cases.

   TIP: If it is unavoidable to route across a gap, the two areas of plane (on either side of the gap) can often be connected together at RF frequencies with a small capacitor or two (100-1000 pF) placed immediately adjacent to the trace and bridging the gap in the plane. This provides an explicit path for the return current to take across the gap to keep the loop area small.

3. If traces are routed over both sides of a ground plane, each will have a return current reflected in the plane below it. If the traces cross each other at right angles, there will be little interaction between the return currents. If the traces are parallel and directly above and below each other, the return current can interact at medium frequencies. It is wise to look at both layers (above and below the plane) to check for possible interactions. Note

that at RF frequencies (about 60 MHz for ½ oz. Cu and 15 MHz for 1 oz. Cu), the return currents will be constrained by the skin effect to the outer surfaces of the ground plane and upper and lower layers will generally not interact.

4. On two layer boards, create a virtual ground plane by filling in the area between traces with copper pour and stitching it up to create a "grid" with no long uninterrupted slots or gaps. This is tricky, but can be very helpful in keeping to a 2-layer board if required. If it is not practical to do this well or the clock frequency is over about 8-10 MHz, think hard about going to a 4 layer. Note: Never allow a section of copper to float. Connect it to the ground plan or leave it out.

5. Differential traces (such as for USB and Ethernet) are run as balanced pairs. This makes them far less susceptible to problems crossing a gap than for single traces since the return current is explicitly routed (as the other half of a pair). It is still not recommended to cross a gap however, as there can still be a common mode signal (which also has a return path). It is very important to preserve the balance by not routing only one side of the pair close to or over a gap or near another trace. The imbalance can give rise to a common mode signal.

6. Add series impedance to a signal where practical. A small resistor (22 to 50 ohms) in series and located at the driver end of the trace is good for reducing reflections and ringing. If a DC impedance is unacceptable, a ferrite bead can be used. It will have very low impedance at low frequency but significant impedance at RF (100-200 MHz). When using a ferrite, be sure to not saturate the material due to too much current. Also, use a material with the desired impedance at the frequency range of interest.

7. Bypass capacitors should be placed as close to the pins that they bypass as practical. Recommended routing is pin to cap then to a via or the power trace. Remember that a low impedance path from the cap back to the chip's ground is essential for proper performance. From an EMI perspective, a lower value cap (0.001 uF to 0.01uF typical) placed closest to the chip followed by a 0.01uF to 0.1uF nearby is good. Remember that the lead inductance (of the cap and the traces routing to it) establish a "self resonant" frequency at which the capacitor will be ineffective. Higher value caps have lower self-resonant frequencies.

   > TIP: Placing a ferrite bead right at the chip which in series with the power which feeds the bypass caps and power pins of the chip can substantially reduce the amount of noise coming from a chip back into the power supply traces or planes. This helps keep noise from the chip localized to the chip. It can also help keep RF interference from getting in via the power lead.

8. Pay close attention to routing for bypass capacitors.. Every capacitor has lead inductance creating a resonant circuit with its own capacitance. This leads to a self-resonance which limits the effective frequency to which a capacitor can effectively provide the bypass capacitor function. Since small surface mount capacitors have very small lead inductance, the PCB routing usually is more important than the SMD caps themselves. For a given trace inductance, the higher the capacitance value, the lower the self-resonant frequency. A 0603 package has a parasitic inductance of about 0.87 nH which leads to a self-resonance of about 18 MHz. Add a short trace and a via and the total might be might

be about 3nH, leading to a self-resonance of 9 MHz. A 1000 pF would be 92MHz and a 100 pF would be 290 MHz. This is where the 100pF to 1000pF range for typical EMI caps arises. This is also why very short traces and vias in parallel are used for RF frequencies. [source: AVX: "Parasitic Inductance of Multilayer Ceramic Capacitors"; Fr = $1/(2\pi*\text{sqrt}(LC))$].

Note: Feed-though style bypass capacitors have much higher self resonant frequencies and are very effective from an EMI perspective. If carefully chosen and correctly routed, a single somewhat higher capacitance feed-through will outperform multi-capacitor options.

9. Chip grounding is extremely important. A very low impedance from the Chip's internal ground to the ground plane is vital to keeping noise level down in the system. Every ground pin should have its own ground connection. *Don't share* GND or bypass capacitor vias. If there is a ground tab or pad on the chip, ground it well and with multiple vias (thermal reliefs are OK so long as they are low impedance (4 spoke).

    TIP: Use copper pour fills to augment the ground in the vicinity of the chip with multiple vias to stitch it to the GND plane. Tie this in with bypass caps if practical. The idea is to have a *very* low impedance ground between the chip and its bypass caps. This is because every time the chip needs a pulse of current to drive on output line to a different state, it needs to pull current from the bypass cap or drive it into the ground path. If there is even a small impedance, the resulting voltage drop during the pulse, the resulting "ground bounce" will be transferred to *every IO pin* on the chip, sending noise pulses all over the PCB.

10. The best place to filter a signal is right at the source (driver), if practical. A series impedance (resistor or ferrite) with a shunt capacitor (to ground) will limit the rise time and peak current. The capacitor should be close to and returned to ground right at the chip. In many cases, this is not practical or sufficient. In this case, a filter on an IO signal right at the connector (board entry/exit point) can be used with the capacitor returned to the shield or clean (connector) ground (if there is a separate one) or the GND plane on only one.

11. If a "clean" area is created, such as an opto-isolated IO zone, it is vital to keep ALL traces which are not isolated and clean from traversing the zone, even briefly. Clean is only clean if nothing contaminates it.

12. A "clean" IO ground (e.g., shield ground) can be created at the board perimeter. If this is done, the area should be wide and should tie into all the mounting features as well as the board shield enclosure. The digital ground plane should not tie directly to this ground except through a small impedance. Note that this assumes that there is an external shield enclosure around the board and that all IO and power has either been shielded or filtered to the shield ground. If this is not the case, it is usually better to tie the ground plane down to all the mounting holes. This amounts to an essentially unshielded design and all connections must be filters (to the GND plane).

13. For high current pulses such as in a switching supply, identify the loop (including through reservoir and filter capacitors) and provide a separate, low impedance path for

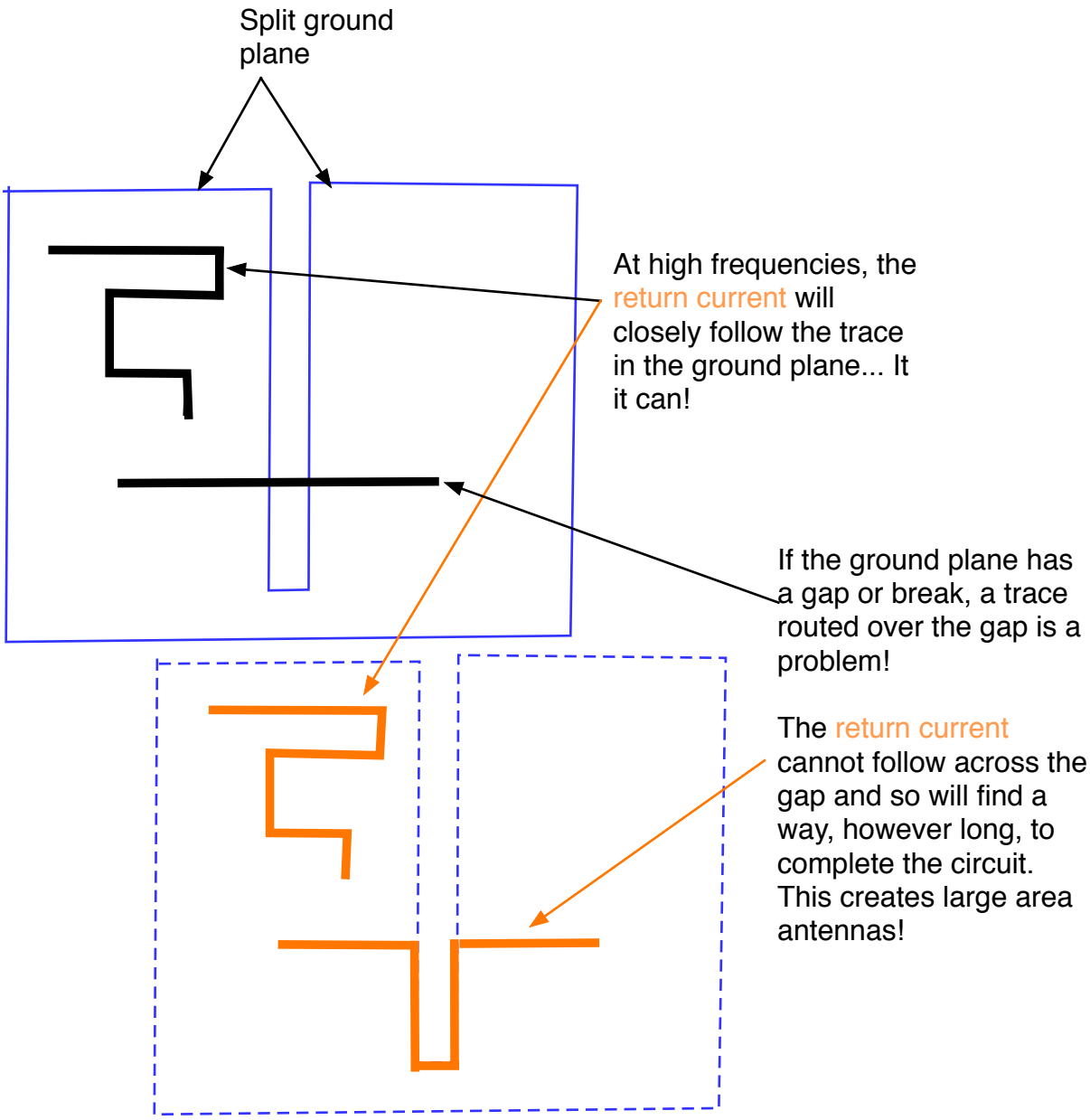
these. Tie to the GND plane carefully, usually at a single point. Following the manufacturer's layout recommendations and notes is usually advised.

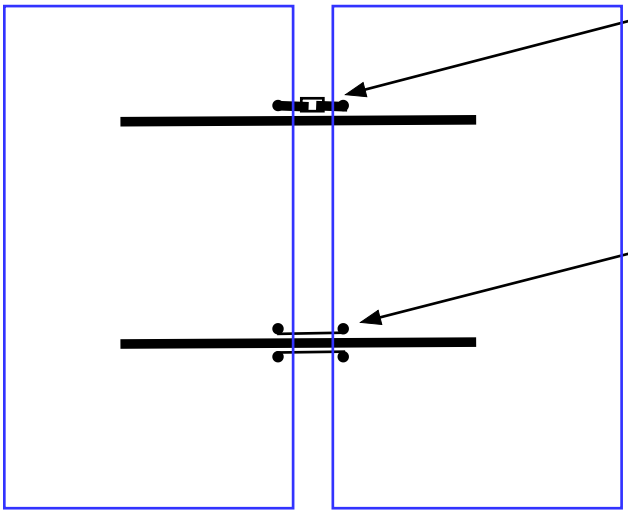
Summary:

- Identify and control the return current paths
- Minimize the loop area
- A good, low RF impedance ground is essential
- Minimize the frequency (including harmonics) as close to the source as practical

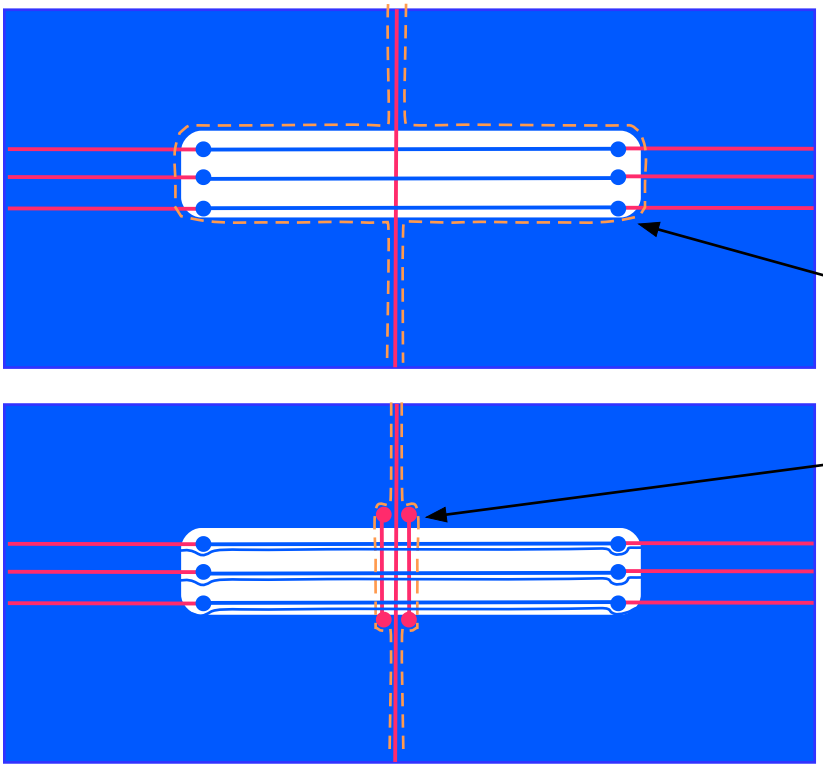
IMPORTANT: These are partial guidelines based on my experience. Each design is unique and there is no assurance that even if properly applied these guidelines will achieve the desired results. They also are considered only from an EMI perspective and have not taken into account any safety or other performance considerations which may apply to a given design.

Appendix - PCB Gaps Drawings:

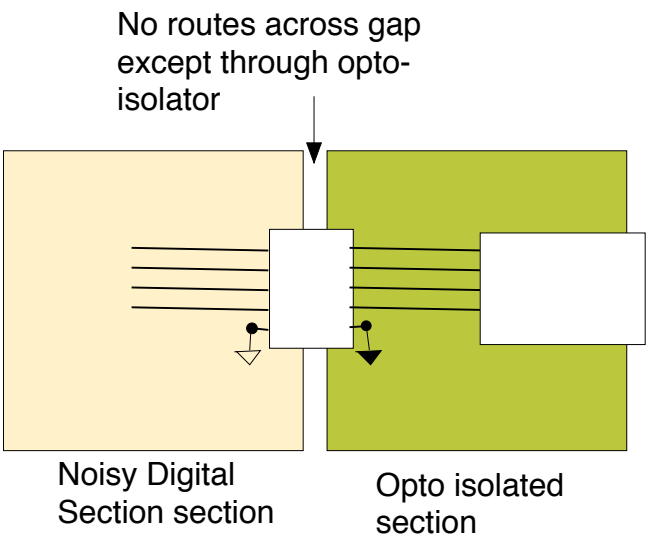




Some options to provide a return path across a gap when routing across it can't be avoided



Some cross over options on 2 layer boards to provide a return path across a necessary gap



Opto-isolated sections can be effective at blocking noise, but no noisy traces can be allowed onto the isolated section. The stray capacitance between the two sides of an isolator are usually very low… about 1 pF (up to 3pF for some). 1 pF has an impedance of about 1600 ohms. Ay 100MHz and 160 ohms at 1GHz. This is enough impedance for good isolation at RF provided that the RF common mode path to clean system ground (e.g., shield) is substantially lower impedance.

The isolated ground can be DC or RF tied (i.e., through capacitors) to a quiet perimeter or Earth ground, depending on system needs. Note that planes should not extend across the gap under the isolated ground and traces must not cross over even fro a short distance… The isolated section must be kept clean of system noise.